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REMARKS

Counsel for the applicants appreciates the courtesy shown during the telephone interview today. The following incorporates a summary of items discussed during the telephone interview.

The applicants appreciate the acknowledgement of the claim for priority under section 119 and the notice of receipt of the certified copies of the priority documents.

Claims 1-16 are pending. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1-16 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,877,112, Iino ("Iino"). The rejection is respectfully traversed for reasons including the following, which are presented by way of example.

Claim 1 recites in combination, for example "a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal; and an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit, wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal." (See also independent claim 9.) Accordingly, the vector address switching circuit causes the CPU to execute different programs in accordance with different (first or second) reset signals, and the interface circuit is reset only by a second reset signal.

Without conceding that Iino discloses any feature of the present invention, Iino is directed to a reset control system and method. According to Iino, FIG. 3, the first reset control section (605) OR-operates first and second reset signals; the OR operation result is output to the CPU core (604) as a first internal reset signal (629) for initializing the CPU core (604) (column 3, lines 55-63). A companion chip (606) has a second reset control section (607) which distributes the external reset signal (626) to a second internal reset signal (627) and second reset signal (628). (Col. 2, line 64 to Col. 3, line 2.)

The office action asserts that Iino, FIG. 3 discloses the invention as claimed. To the contrary, Iino fails to teach or suggest the invention, as recited, when the claims are considered as a whole.

The office action refers to Iino, column 2, lines 55-67 and column 3, lines 1-6 as teaching first and second reset signals and executing different programs (user and monitor) by outputting different vector addresses of programs in correspondence to the reset signals; and column 11, lines 43-47 as teaching well known art regarding reset signals. The examiner explained during the interview that the combination of first and second reset signals in Iino, FIG. 3 is considered to correspond to the recited "vector address switching circuit" which outputs different vector addresses to the CPU.

In Iino, two reset signals 526, 528 are applied to and OR-operated by a control section 605 (col. 3, lines 36-39), which in turn resets a CPU 604 by a single reset signal 629. This corresponds to two reset signals RST1, RST2 and an OR circuit 31, which reset CPU 22, illustrated in FIG. 1 of the present application. In each case, it is only possible to reset the CPU, and the CPU starts the same program. The CPU cannot recognize which one of the different reset signals is used, and hence cannot differentiate programs to execute after being thus reset.

According to the claims, besides the above reset circuit and operation, a "vector address switching circuit" is included to output different vector addresses to the CPU, corresponding respectively to the different reset signals RST1, RST2. Consequently, the CPU is enabled to recognize which one of the different reset signals is resetting it, and will execute different programs by referring to the different respective vector addresses.

Iino absolutely fails to teach or suggest, for example, "***a vector address switching circuit*** configured for outputting ***a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal***, and for outputting ***a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal***." (See, e.g., claims 1, 9.) To the contrary, although Iino discloses different reset signals, Iino fails to teach or suggest anything about outputting different vector addresses from a vector address switching circuit to selectively switch based on the reset signal to different programs to be executed by a CPU.

Iino fails to teach or suggest, for example, these elements recited in amended independent claims 1 and 9. It is respectfully submitted therefore that claims 1 and 9 are patentable over Iino.

For at least these reasons, the combination of features recited in independent claims 1 and 9, when interpreted as a whole, is submitted to patentably distinguish over the references of record. In addition, Iino clearly fails to show other recited elements as well.

With respect to the rejected dependent claims, applicant respectfully submits that these claims are allowable not only by virtue of their dependency from independent claims 1 and 9, but also because of additional features they recite in combination.

Applicants respectfully submit that, as described above, the cited art does not show or suggest the combination of features recited in the claims. Applicants do not concede that the

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cited art shows any of the elements recited in the claims. However, applicants have provided specific examples of elements in the claims that are clearly not present in the cited art.

Applicants strongly emphasize that one reviewing the prosecution history should not interpret any of the examples applicant has described herein in connection with distinguishing over the cited art as limiting to those specific features in isolation. Rather, for the sake of simplicity, applicants have provided examples of why the claims described above are distinguishable over the cited references.

In view of the foregoing, the applicants submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,

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